**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) A switch circuit comprising:

at least two input terminals and one output terminal,

first switches, each first switch comprising a first and second port, said first switches being electronically switchable between a first state, where there is a high insertion loss between the corresponding first and second ports, and a second state, where there is a low insertion loss between the corresponding first and second ports, where each of the input terminals is connected to a first port of a respective one of said first switches, ~~and~~

a second switch with at least two branch ports and a common port coupled to said output terminal, said second switch electronically switchable between different states, where in each state the insertion loss between one branch port and the common port is low~~, while~~ and the insertion loss between any other branch port and the common port ~~and the other branch port~~ is high, where each of the branch ports is connected to a second port of one of said first switches; and

a control circuit comprising a control terminal, a first driver circuit and a second driver circuit, where the first driver circuit and the second driver circuit are operably connected to the control terminal, the first driver circuit provides an in-phase voltage signal to drive one of the first switches, and where the second driver circuit provides an

inverted voltage signal to drive another of the first switches, wherein the in-phase voltage signal and the inverted voltage signal are generated from a signal provided at the control terminal,

wherein said first switches are each implemented using two anti-parallel PIN-diodes in series connection between first and second ports, and a driver terminal is connected between the diodes.

2. (canceled)

3. (canceled)

4. (previously presented) Circuit according to claim 1, where the first switches are comprised of discrete electronic parts.

5. (previously presented) Circuit according to claim 1, where the second switch is an integrated circuit.

6. (currently amended) Circuit according to claim 1, where ~~a~~ the control circuit is provided to synchronously control said first switches and said second switch.

7. (canceled)

8. (currently amended) Circuit according to claim 6, where the control circuit is

connected to an ~~I2C~~ $I^2C$ transceiver.

9. (previously presented) A receiver circuit for receiving a radio frequency signal, comprising at least two radio frequency input terminals, a tuner circuit for receiving radio frequency signals at an input, and for generating baseband signals, and a switch circuit according to claim 1, where the input terminals are connected to the radio frequency inputs and the output terminal is connected to the input of the tuner.

10. (new) A receiver circuit for receiving a radio frequency signal, the receiver circuit comprising:

at least two radio frequency input terminals;

a tuner circuit for receiving radio frequency signals at an input, and for generating baseband signals, wherein the tuner circuit includes an $I^2C$ transceiver; and

a switch circuit comprising:

at least two input terminals and one output terminal,

first switches, each first switch comprising a first and second port, said first switches being electronically switchable between a first state, where there is a high insertion loss between the corresponding first and second ports, and a second state, where there is a low insertion loss between the corresponding first and second ports, where each of the input terminals is connected to a first port of a respective one of said first switches, and

a second switch with at least two branch ports and a common port coupled to said output terminal, said second switch electronically switchable between different

states, where in each state the insertion loss between one branch port and the common port is low and the insertion loss between any other branch port and the common port is high, where each of the branch ports is connected to a second port of one of said first switches,

where the input terminals are connected to the radio frequency inputs and the output terminal is connected to the input of the tuner and the $I^2C$ transceiver receives commands via an $I^2C$ bus and controls the switch circuit.

11. (new) The receiver circuit of claim 10, where the first switches are implemented using PIN diodes.

12. (new) The receiver circuit of claim 11, where first switches are implemented using two anti-parallel PIN-diodes in series connection between first and second ports, and a driver terminal is connected between the diodes.

13. (new) The receiver circuit of claim 10, where the first switches are comprised of discrete electronic parts.

14. (new) The receiver circuit of claim 10, where the second switch is an integrated circuit.

15. (new) The receiver circuit of claim 10, where a control circuit is provided to synchronously control said first switches and said second switch.

16. (new) The receiver circuit of claim 10, where a control circuit is provided comprising a control terminal and at least two driver circuits, where a first driver circuit provides an in-phase voltage signal to drive one of the first switches, and where the second driver circuit provides an inverted voltage signal to drive another of the first switches.

17. (new) A switch circuit comprising:

at least two input terminals and one output terminal;

first switches, each first switch comprising a first and second port, said first switches being electronically switchable between a first state, where there is a high insertion loss between the corresponding first and second ports, and a second state, where there is a low insertion loss between the corresponding first and second ports, where each of the input terminals is connected to a first port of a respective one of said first switches;

a second switch with at least two branch ports and a common port coupled to said output terminal, said second switch electronically switchable between different states, where in each state the insertion loss between one branch port and the common port is low and the insertion loss between any other branch port and the common port is high, where each of the branch ports is connected to a second port of one of said first switches; and

a control circuit comprising a control terminal, a first driver circuit, a second driver circuit, and a third driver circuit, where the first driver circuit provides an in-phase voltage signal to drive one of the first switches, where the second driver circuit provides an inverted voltage signal to drive another of the first switches, wherein the in-phase

voltage signal and the inverted voltage signal are generated from a signal provided at the control terminal, and where the third driver circuit provides a switching voltage signal to drive the second switch, wherein the third driver circuit is a resistive divider network and the switching voltage signal is obtained from the in-phase voltage signal.

18. (new) The switch circuit of claim 17, where the first switches are implemented using PIN diodes.

19. (new) The switch circuit of claim 18, where first switches are implemented using two anti-parallel PIN-diodes in series connection between first and second ports, and a driver terminal is connected between the diodes.

20. (new) The switch circuit of claim 17, where a control circuit is provided to synchronously control said first switches and said second switch.

21. (new) The switch circuit of claim 17, where a control circuit is provided comprising a control terminal and at least two driver circuits, where a first driver circuit provides an in-phase voltage signal to drive one of the first switches, and where the second driver circuit provides an inverted voltage signal to drive another of the first switches.

22. (new) The switch circuit of claim 20, where the control circuit is connected to an $I^2C$ transceiver.

23. (new) A receiver circuit for receiving a radio frequency signal, comprising at least two radio frequency input terminals, a tuner circuit for receiving radio frequency signals at an input, and for generating baseband signals, and a switch circuit according to claim 17, where the input terminals are connected to the radio frequency inputs and the output terminal is connected to the input of the tuner.